unpatentable over Beaudoin. Applicant respectfully traverses the rejections and requests reconsideration.

Criteria for a Rejection under 35 U.S.C. § 102

The criteria for a rejection under 35 U.S.C. § 102 has been clearly defined by the courts and confirmed by the U.S. Patent and Trademark Office. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Criteria for a Rejection under 35 U.S.C. § 103(a)

The U.S. Patent and Trademark Office has set forth a methodology for establishing a *prima facie* case of obviousness. Specifically, three basic criteria must be met.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

See MPEP 706.02 (j).

Overview of Reason for Traversal

All the independent claims were rejected under 35 U.S.C. § 102 (e).

However, Examiner has failed to show that each and every element set forth

in the independent claims is found either expressly or inherently in Beaudoin.

Below, Applicant clearly and unambiguously points out subject matter

within each independent claim that is not disclosed or suggested by

Beaudoin. On the basis of this, Applicant believes all the claims are

patentable over Beaudoin, whether considered alone or in combination with

Hans.

Brief Description of Beaudoin

Beaudoin discloses a network address matching circuit and method. A

circuit 200, preferably implemented on a single chip, consists of Ethernet

media access control (MAC) blocks 1201,1221,1241, a first-in first-out (FIFO)

RAM block 1301, a DRAM interface block 1421, a queue manager block 1401,

an address compare block 150, an EEPROM interface block 801, a network

monitoring multiplexer (mux) block 1601, an LED interface block 1801, a DIO

interface block 1701, an external address interface block 184 and network

statistics block 1681. Each of the MACS 1201, 1221, 1241 is associated with a

communications port 116,117,118 of the circuit 200; thus, the circuit 200 has

fifteen available communications ports for use in a communications system

of the present invention. See column 14, lines 47 through 65.

Brief Description of Han

Han discloses an apparatus and method for serial data communication utilizing general microcomputer.

Discussion of Independent Claim 1

Independent claim 1 sets out a chip for incorporation within a network device connectable to a computer network. The chip includes a media access controller, a host interface and an embedded processor.

The embedded processor is between the host interface and the media access controller. The embedded processor is programmable to function as a manageability web server, communicate with the host interface and obtain manageability information about the network device. The embedded processor further is programmable to send the manageability information to the media access controller for transmission over the computer network. None of this functionality is disclosed or suggested by Beaudoin, whether considered alone or in combination with Han.

The Examiner has asserted that Circuit 200 of Beaudoin includes an embedded processor. Examiner appears to be making this assertion based on the statement by Beaudoin at column 15, lines 5 through 7: "More particularly, this consolidation results in the elimination of the need for an external CPU to control, or coordinate control, of all these functions."

However, this statement in Beaudoin does not specifically state that Circuit 200 includes an embedded processor, but only indicates that there is

no need for an external CPU to control or coordinate control of functions performed by circuit 200. ,

Applicant notes that claim 1 does not merely state that the chip includes an embedded processor. Claim 1 also particularly points out various features of the embedded processor. Claim 1 indicates the embedded processor is between the host interface and the media access controller. The embedded processor is programmable to function as a manageability web server, communicate with the host interface and obtain manageability information about the network device. The embedded processor further is programmable to send the manageability information to the media access controller for transmission over the computer network. None of this functionality is disclosed or suggested by Beaudoin.

Applicant notes that Beaudoin does not even specifically indicate that circuit 200 includes an embedded processor. Examiner is apparently only inferring the existence of an embedded processor within Beaudoin. However, nothing in Beaudoin could be take to infer, for example, that any embedded processor within circuit 200 would be programmable to function as a manageability web server, as set out in claim 1 of the present application. Beaudoin does not even mention the web or the internet.

As discussed above for a rejection under 35 U.S.C. § 102: "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, supra. It is clear that Beaudoin does not give any detail about any embedded processor that may

be within circuit 200. It is inconceivable that if circuit 200 were to include

an embedded processor, it would have the functionality performed by the

embedded processor set out in claim 1 of the present application. Claim 1,

therefore, is clearly not anticipated by nor unpatentable over Beaudoin.

Discussion of Independent Claim 13

Independent claim 13 sets out a network device. The network device

includes a chip. The chip includes a media access controller, an interchip

communications interface and an embedded processor.

Non-volatile memory is programmed with a plurality of executable

instructions. The instructions, when executed, instructs the embedded

processor to function as a manageability web server, communicate with the

interchip communications means to obtain manageability information

about the compliant device, and send the manageability information to the

media access controller for transmission over the computer network. This

functionality is not disclosed or suggested by the cited art.

The Examiner has asserted that Circuit 200 of Beaudoin includes an

embedded processor. As discussed above, Examiner appears to be making

this assertion based on the statement by Beaudoin at column 15, lines 5

through 7: "More particularly, this consolidation results in the elimination of

the need for an external CPU to control, or coordinate control, of all these

functions."

However, this statement in Beaudoin does not specifically state that Circuit 200 includes an embedded processor, but only indicates that there is no need for an external CPU to control or coordinate control of functions performed by circuit 200.

Applicant notes that claim 13 does not merely state that the chip includes an embedded processor. Claim 13 also particularly points out various features of the embedded processor. Claim 13 indicates the embedded processor is instructed to function as a manageability web server, communicate with the interchip communications means to obtain manageability information about the compliant device, and send the manageability information to the media access controller for transmission over the computer network. None of this functionality is disclosed or suggested by Beaudoin.

Applicant notes that Beaudoin does not even specifically indicate that circuit 200 includes an embedded processor. Examiner is apparently only inferring the existence of an embedded processor within Beaudoin. However, nothing in Beaudoin could be take to infer, for example, that any embedded processor within circuit 200 would be programmable to function as a manageability web server, as set out in claim 13 of the present application. Beaudoin does not even mention the web or the internet.

As discussed above for a rejection under 35 U.S.C. § 102: "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, supra. It is clear that

Beaudoin does not give any detail about any embedded processor that may be within circuit 200. It is inconceivable that if circuit 200 were to include an embedded processor, it would have the functionality performed by the embedded processor set out in claim 13 of the present application. Claim 13, therefore, is clearly not anticipated by nor unpatentable over Beaudoin.

Discussion of Independent Claim 23

Independent claim 23 sets out a system. The system includes a network device. The network device includes a chip. The chip includes a media access controller and an embedded processor programmed to function as an HTTP manageability web server. This functionality is not disclosed or suggested by the cited art.

The Examiner has asserted that Circuit 200 of Beaudoin includes an embedded processor. As discussed above, Examiner appears to be making this assertion based on the statement by Beaudoin at column 15, lines 5 through 7: "More particularly, this consolidation results in the elimination of the need for an external CPU to control, or coordinate control, of all these functions."

However, this statement in Beaudoin does not specifically state that Circuit 200 includes an embedded processor, but only indicates that there is no need for an external CPU to control or coordinate control of functions performed by circuit 200.

Applicant notes that claim 23 does not merely state that the chip includes an embedded processor. Claim 23 also particularly points out various features of the embedded processor. Claim 23 indicates the embedded processor is programmed to function as an HTTP manageability web server. This functionality is disclosed or suggested by Beaudoin.

Applicant notes that Beaudoin does not even specifically indicate that circuit 200 includes an embedded processor. Examiner is apparently only inferring the existence of an embedded processor within Beaudoin. However, nothing in Beaudoin could be take to infer, for example, that any embedded processor within circuit 200 is programmed to function as an HTTP manageability web server, as set out in claim 23 of the present application. Beaudoin does not even mention the web or the internet.

As discussed above for a rejection under 35 U.S.C. § 102: "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, supra. It is clear that Beaudoin does not give any detail about any embedded processor that may be within circuit 200. It is inconceivable that if circuit 200 were to include an embedded processor, it would have the functionality performed by the embedded processor set out in claim 23 of the present application. Claim 23, therefore, is clearly not anticipated by nor unpatentable over Beaudoin.

Conclusion

Applicant believes that the present Application is in condition for allowance and favorable action is respectfully requested.

Respectfully submitted,
DAVE GOH, ET AL.

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